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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,307	07/01/2003	Akihiro Matsuda	10873.352USRE	3972

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/611,307	MATSUDA ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 15-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/209,214.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 03/26/07 has been entered.

Reissue Applications

2. Claims 1-5 and 15-18 are rejected under 35 U.S.C. 251 as being based upon a defective reissue declaration. See 37 CFR 1.175.

A. The reissue oath/declaration filed with this application is defective because it fails to identify at least one error that is relied upon to support the reissue application. See 37 CFR 1.175(a)(1) and MPEP § 1414.

B. The reissue oath/declaration filed on 3/26/07 is defective because it is not signed. See 37 CFR 1.175(a)(1) and MPEP § 1414. It is noted that in the 3/26/07 reissue oath applicant correctly notes that the subject matter of figure 5 and column 5 (identified in the specification as the "second embodiment") was not claimed in the '214 patent. The reissue oath/declaration filed on 3/26/07 thus identifies at least one error that may be relied upon to support the reissue application. It is noted that on 6/17/05 Petitions Branch determined that applicant is entitled to a filing date of 07/01/03, less than two years after the '214 patent issued.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-5 are rejected under 35 U.S.C.§ 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 1-5 require the combined limitations of 1) a plurality of semiconductor elements surrounded by a plurality dummy elements; and 2) the limitation that the semiconductor elements be transistors.

Applicants' second and fourth embodiments, as filed, each include the limitation of a plurality of semiconductor elements 32 or 52 surrounded by a plurality of dummy elements 33 or 53. Note figures 5 and 6. But each and every one of the semiconductor elements 32 or 52 must be capacitors. Note column 5 lines 15-50, and column 6 lines 10-62.

Applicants' fifth embodiment, as filed, includes the limitation of a plurality of transistor elements 121 adjacent a single dummy element 122. Note column 7 lines 1-44. But there is but a single (not a plurality of) dummy element 122 in Applicants' fifth embodiment, and it does not surround the plurality of transistor elements 121. Note figure 13.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 15-18 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recites the limitations "the semiconductor elements" in line 7, and "the dummy semiconductor elements" in line 8. There is insufficient antecedent basis for these limitations in the claim. The only previous mention of any such things are "a semiconductor element" in line 4, and "a dummy semiconductor element." "A semiconductor element" can provide antecedent basis for only one (not all) of the "elements" referred to in line 7.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over YAMASAKI ET AL. (5,396,100) in view of TAKASU (5,361,224).

Yamasaki et al. discloses a semiconductor device comprising a substrate 1, and a semiconductor element area (B region), including a plurality of semiconductor elements

4, on the substrate 1, and a dummy semiconductor element area (A region), including a plurality (note particularly column 53 lines 8-35) of dummy semiconductor elements 4D1-4D4, on the substrate 1, the semiconductor element area (B region) being surrounded by the dummy semiconductor element area (A region) (and thus the electrode 7 is surrounded by the dummy electrode 7D1, 7D2, etc); each of the semiconductor elements 4 including a first dielectric layer 6 and an electrode 7 on the first dielectric layer 6; each of the dummy semiconductor elements 4D1-4D4 including a second dielectric layer 6 (laid down at the same time as, and bearing the same part #, as first dielectric layer 6) composed of the same dielectric material as the first dielectric layer 6; and a dummy electrode 7D1, 7D2, etc, composed of the same electrically conductive material as the electrode 7, on the second dielectric layer 6, wherein each of the dummy semiconductor elements 4D1-4D4 is located so that a space F3 between the electrode 7 and the dummy electrode 7D1, 7D2, etc is in a predetermined range between 0.3 μm and 14 μm; wherein each of the semiconductor elements 4 is a transistor (Qd1, Qd2, Qp1, or Qp2) in which the electrode 7 works as a gate electrode 7 of the transistor (Qd1, Qd2, Qp1, or Qp2). Note figures 9A-9D, column 38 lines 54-57, and columns 52-54 of Yamasaki et al.

Yamasaki et al. discloses that the first and second dielectric layers are composed of the same material, but Yamasaki et al. does not disclose that that same material is a ferroelectric material. However, Takasu discloses a semiconductor device having

transistors 24-27 with $Pb(Zr_{1-x}Ti_x)O_3$ ferroelectric dielectric layers 23. Note figures 3 and 4 and column 6 lines 27-52 of Takasu. Takasu explains, see column 4 lines 1-10, that the ferroelectric dielectric layers allow memory arrays utilizing gate dielectrics formed from such material to retain data in the event of a power interruption. Therefore, it would have been obvious to a person having skill in the art to replace the dielectric layers of Yamasaki et al.'s semiconductor device with the $Pb(Zr_{1-x}Ti_x)O_3$ ferroelectric dielectric layers such as taught by Takasu in order to utilize a dielectric layer that exhibits hysteresis to thus allow data retention in the event of a power failure.

B. Claims 15-18 rejected under 35 U.S.C. 103(a) as being unpatentable over TAKAISHI (5,913,150) in view of TAKASU (5,361,224).

Takaishi discloses a semiconductor device comprising a substrate 1 and a multilayer 7-8-11-13-14-14'-15-15'-20-21-22 formed on the substrate 1, the multilayer 7-8-11-13-14-14'-15-15'-20-21-22 comprising a semiconductor element 12-13-14-15 and a dummy semiconductor element 21-14-15-20-22, and a semiconductor element area A1 on the substrate 1, which includes a plurality of the semiconductor elements 12-13-14-15, and a dummy area A1 on the substrate 1, which includes a plurality of the dummy semiconductor elements 21-14-15-20-22, the semiconductor element area A1 being surrounded by the dummy area A1; wherein the semiconductor element 12-13-14-15 includes a capacitor 13-14-15 which is comprised of a bottom electrode 13, a first dielectric layer 14 on the bottom electrode 13 and a top electrode 15 on the first

dielectric layer 14; wherein the dummy semiconductor element 21-14-15-20-22 includes a dummy capacitor 21-14-15 which is comprised of a dummy bottom electrode 21, a second dielectric layer 14' on the dummy bottom electrode 21 and a dummy top electrode 15' on the second dielectric layer 14', wherein the dummy semiconductor element 21-14-15-20-22 is located so that a space between the electrode and the dummy electrode is in a predetermined range. Note figures 6H-6M column 6 lines 52-60, and column 7 lines 1-30 of Takaishi.

Takaishi discloses that the first 14 and second 14' dielectric layers are composed of the same material, but Takaishi does not disclose that that same material is a ferroelectric material. However, Takasu discloses a semiconductor device having capacitors 3-4 with ferroelectric dielectric layers (such as the $Pb(Zr_{1-x}Ti_x)O_3$ found in 4,873,664, to which Takasu refers at column 1 line 12) Note figures 12 and 13 and columns 1 and 2 of Takasu. Takasu explains, see column 4 lines 1-10, that the ferroelectric dielectric layers allow memory arrays utilizing capacitors formed from such material to retain data in the event of a power interruption. Therefore, it would have been obvious to a person having skill in the art to replace the dielectric layers of Takaishi's semiconductor device with the $Pb(Zr_{1-x}Ti_x)O_3$ ferroelectric dielectric layers such as taught by Takasu in order to utilize a dielectric layer that exhibits hysteresis to thus allow data retention in the event of a power failure.

Claim 17 recites a range limitation on the "remnant polarization" of the capacitor. In accordance with applicant's specification, the examiner interprets "remnant polarization" as the lower limit on the polarization of the ferroelectric material of the first dielectric layer, when one takes reasonable care to wind the polarization down through a fair number of hysteresis loops, as is commonly done to reduce residual polarization in a ferroelectric capacitor, by those practicing the ferroelectric capacitor art. There is at least a reasonable basis for believing that the capacitor of device suggested by Takaishi and Takasu is inherently capable of being run through hysteresis wind-down to reach the claimed "remnant polarization," namely, the fact that the device suggested by Takaishi and Takasu is structurally identical to the invention described by Applicants. *See In re Spada*, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990), (prior art polymers anticipated claimed polymers despite the fact that claims recited "tackiness" while prior art reference described the polymers as "hard and abrasion resistant"), MPEP § 2112 (part III) (a rejection under 35 U.S.C. § 102/103 can be made when the prior art product seems to be identical except that the prior art is silent as to an inherent characteristic), and MPEP § 2112.01 (when the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent).

The applicant's claims 15-18 do not distinguish over the Takaishi and Takasu references regardless of the process used to form the multilayer, electrode, dummy

electrode, first dielectric layer, second dielectric layer bottom electrode, and dummy bottom electrode, because only the final product is relevant, not the recited process of forming a dielectric film for the first dielectric laver and the second dielectric layer; forming an electrically conductive film on the dielectric film; and etching the electrically conductive film so as to form the electrode and the dummy electrode, etching the dielectric film so as to form the first dielectric layer and the second dielectric layer. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d 1097 (Fed. Cir, 2006) ("While the process set forth in the product-by-process claim may be new, that novelty can only be captured by obtaining a process claim.")

Note that when "product by process" claiming is used to describe one or more limitations of a claimed product, the limitations so described are limitations of the claimed product per se, no matter how said product is actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims

or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

The Federal Circuit recently revisited the question of whether a "product by process" claim can be anticipated by a reference that does not recite said process. See *SmithKline Beecham Corp. v. Apotex Corp.*, 78 USPQ2d at 1099-1101. The Federal Circuit cited with approval this Office's current statement of the law, found in MPEP § 2113:

> [Even] though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.

Id. at 1101. The Federal Circuit held this statement to be consistent with its own views on this topic, as well as various Supreme Court rulings, notably *Gen. Elec. Co. v. Wabash Appliance Corp.*, 304 U.S. 364, 373 (1938) ("Although in some instances a claim may validly describe a new product with some reference to the method of production, a patentee who does not distinguish his product from what is old except by reference, express or constructive, to the process by which he produced it, cannot secure a monopoly on the product by whatever means produced."). Id.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

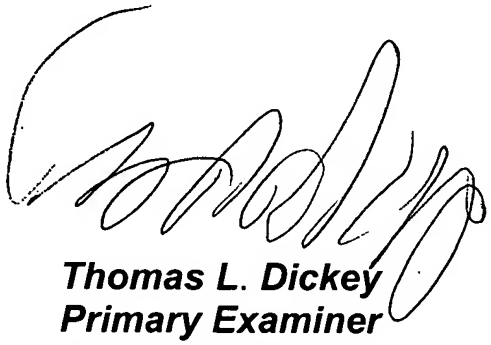
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Primary Examiner
Art Unit 2826